## SYSTEM AND METHOD FOR EXECUTING VARIABLE LATENCY
## LOAD OPERATIONS IN A DATA PROCESSOR

## ABSTRACT OF THE DISCLOSURE

There is disclosed a data processor that executes variable

5      latency load operations using bypass circuitry that allows load

word operations to avoid stalls caused by shifting circuitry. The

processor comprises: 1) an instruction execution pipeline

comprising N processing stages, each of the N processing stages for

performing one of a plurality of execution steps associated with a

10     pending instruction being executed by the instruction execution

pipeline; 2) a data cache for storing data values used by the

pending instruction; 3) a plurality of registers for receiving the

data values from the data cache; 4) a load store unit for

transferring a first one of the data values from the data cache to

15     a target one of the plurality of registers during execution of a

load operation; 5) a shifter circuit associated with the load store

unit for shifting the first data value prior to loading the first

data value into the target register; and 6) bypass circuitry

associated with the load store unit for transferring the first data

20     value from the data cache directly to the target register without

processing the first data value in the shifter circuit.